[What is claimed is:]

1. A method of driving a liquid crystal display comprising a liquid crystal display panel having pixels arranged in a matrix type, a gate driver for applying a scanning signal to gate lines of the liquid crystal display panel, and a data driver for supplying a picture data to data lines of the liquid crystal display panel, and

comprising the steps of:

applying a clock pulse to the gate driver;

applying first to third gate output enable signals to the gate driver; and

applying a scanning pulse to two gate lines during one period of the clock pulse.

2. The method according to claim 1, wherein the data driver supplies the picture data to the data lines when the scanning pulse is applied to a first gate line of the two gate lines, and supplies a black data to the data lines when the scanning pulse is applied to a second gate line of the two gate lines.

3. The method according to claim 1, wherein the data driver supplies a black data to the data lines when the scanning pulse is applied to a first gate line of the two gate lines, and supplies the picture data to the data lines when the scanning pulse is applied to a second gate line of the two gate lines.

4. The method according to claim 1, wherein the first gate output enable signal is applied to the (3i+1)th gate lines (wherein i is 0 or an integer), the second gate output enable signal is applied to the (3i+2)th gate lines, and the third gate output enable signal is applied to the (3i+3)th gate lines.

5. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+1)th gate lines during one period of the clock signal;

applying the scanning pulse to the (3i+2)th gate lines being spaced, by a desired line, from the (3i+1)th gate lines when the scanning pulse is applied to the (3i+1)th gate lines;

maintaining the first gate output enable signal at a high state during a half period of the clock signal when the scanning pulse is applied to the (3i+1)th gate lines; and

maintaining the second gate output enable signal at a high state in such a manner to be alternated with the first gate output enable signal when the scanning pulse is applied to the (3i+2)th gate lines.

6. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+2)th gate lines during one period of the clock signal;

applying the scanning pulse to the (3i+3)th gate lines being spaced, by a desired line, from the (3i+2)th gate lines when the scanning pulse is applied to the (3i+2)th gate lines;

maintaining the second gate output enable signal at a high state during a half period of the clock signal when the scanning pulse is applied to the (3i+2)th gate lines; and

maintaining the third gate output enable signal at a high state in such a manner to be alternated with the second gate output enable signal when the scanning pulse is applied to the (3i+3)th gate lines.

7. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+3)th gate lines during one period of the clock signal;

applying the scanning pulse to the (3i+1)th gate lines being spaced, by a desired line, from the (3i+3)th gate lines when the scanning pulse is applied to the (3i+3)th gate lines;

maintaining the third gate output enable signal at a high state during a half period of the clock signal when the scanning pulse is applied to the (3i+3)th gate lines; and

maintaining the first gate output enable signal at a high state in such a manner to be alternated with the third gate output enable signal when the scanning pulse is applied to the (3i+1)th gate lines.

8. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+1)th gate lines during one period of the clock signal;

applying the scanning pulse to the (3i+3)th gate lines being spaced, by a desired line, from the (3i+1)th gate lines when the scanning pulse is applied to the (3i+1)th gate lines;

maintaining the first gate output enable signal at a high state during a half period of the clock signal when the scanning pulse is applied to the (3i+1)th gate lines; and

maintaining the third gate output enable signal at a high state in such a manner to be alternated with the first gate output enable signal when the scanning pulse is applied to the (3i+3)th gate lines.

9. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+2)th gate lines during one period of the clock signal;

applying the scanning pulse to the (3i+1)th gate lines being spaced, by a desired line, from the (3i+2)th gate lines when the scanning pulse is applied to the (3i+2)th gate lines;

maintaining the second gate output enable signal at a high state during a half period of the clock signal when the scanning pulse is applied to the (3i+2)th gate lines; and

maintaining the first gate output enable signal at a high state in such a manner to be alternated with the second gate output enable signal when the scanning pulse is applied to the (3i+1)th gate lines.

10. The method according to claim 4, further comprising the steps of:

applying the scanning pulse to the (3i+3)th gate lines during one period of the clock signal;

applying the scanning pulse to the (3i+2)th gate lines being spaced, by a desired line, from the (3i+3)th gate lines when the scanning pulse is applied to the (3i+3)th gate lines;

maintaining the third gate output enable signal at a high state during a half period of the clock signal when the scanning pulse is applied to the (3i+3)th gate lines; and

maintaining the second gate output enable signal at a high state in such a manner to be alternated with the third gate output enable signal when the scanning pulse is applied to the (3i+2)th gate lines.